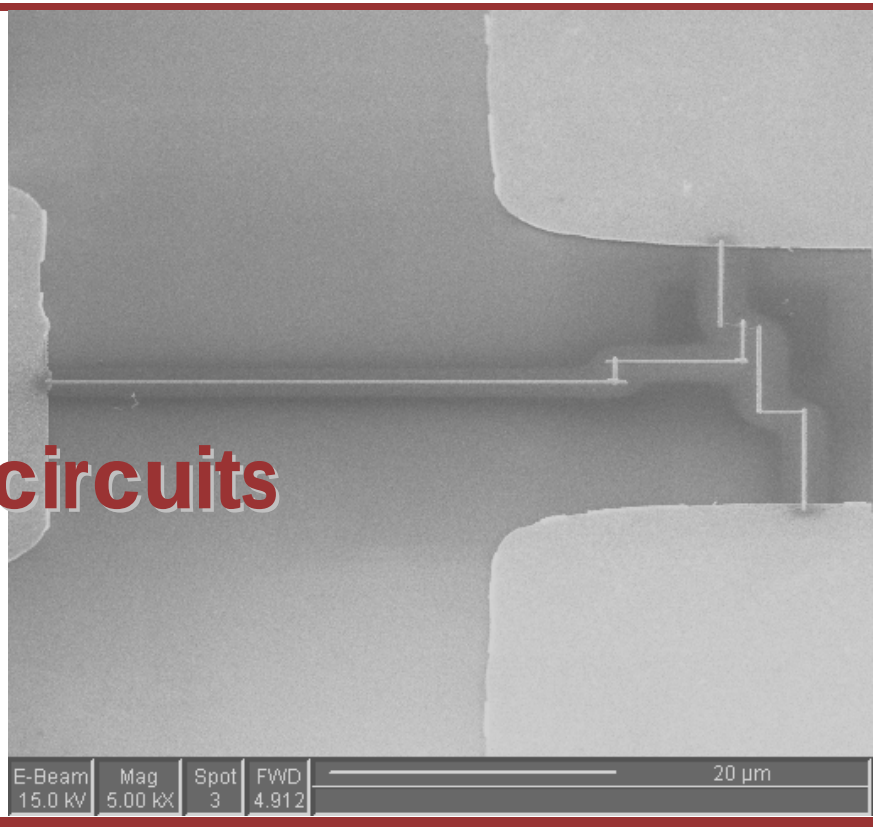
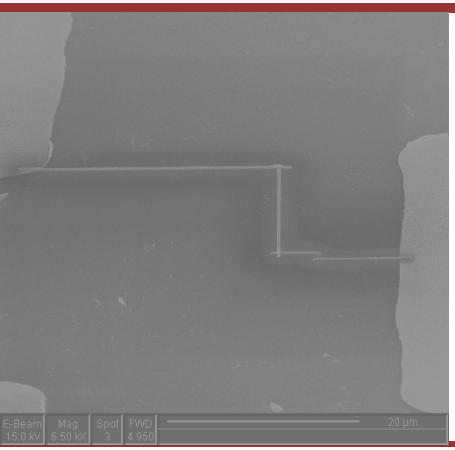
Fab-in-a-Box: Direct-write-Nanocircuits



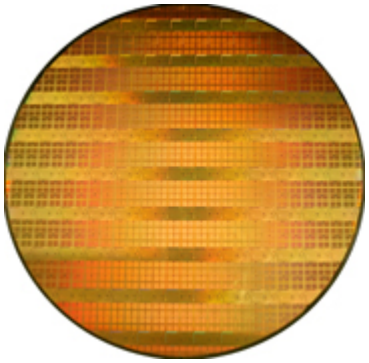


Jaebum Joo and Joseph M. Jacobson

Molecular Machines, Media Lab

Massachusetts Institute of Technology, Cambridge, MA

Avogadro number transistors?



Intel produces ~1200 wafers/day

(Each wafer contains ~10^{11} transistors)

→ 10^{17} transistors / yr

Entire world may be able to fabricate ~10^{18} transistors /yr

→ $10^{18} << 10^{23}$

Moore's 2nd law

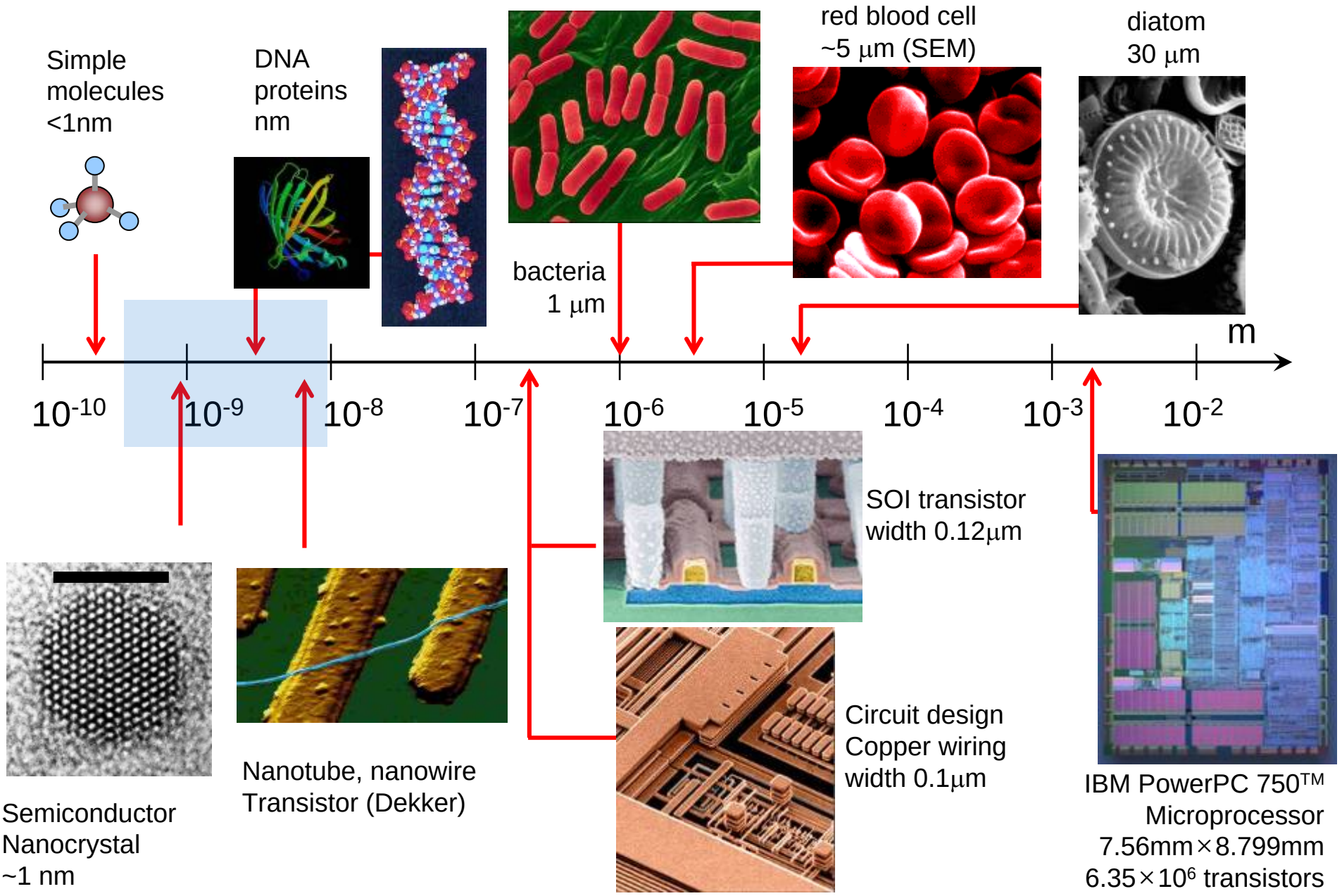
Chip density doubles, cost to set up manufacturing doubles.

Difficult challenges:

1. How to increase the fabrication speed?
2. How to increase the complexity/cost ?

What is the method to approach this Avogadro limit in fabrication?

Complexity comparison (Biology vs. current Fab)

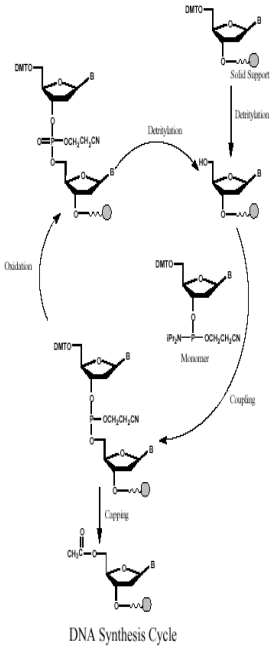


DNA Synthesis

Chemical Synthesis
(Solid Phase Synthesis)

Error Rate:
1: 10^2

300 Seconds
Per step

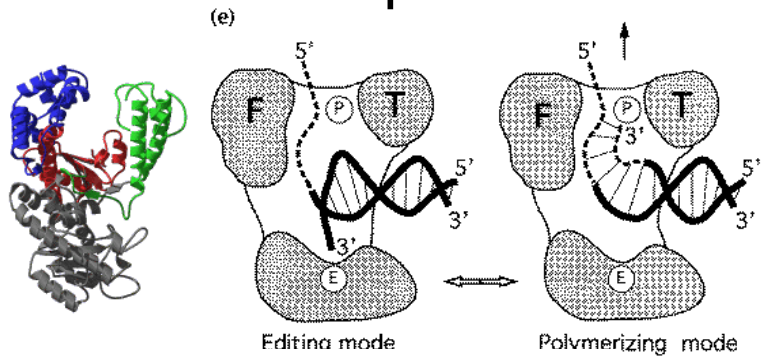


DNA Synthesis Cycle

Biological Synthesis
(Error Correcting Polymerase)

Error Rate:
1: 10^6

100 Steps
per second




```
          T
5′-C T G C A T G C
   | | | | | | | |
3′-G A C G T A C G G C T A G C
          ↓
5′-C T G C A T G C
   | | | | | | | |
3′-G A C G T A C G G C T A G C
```

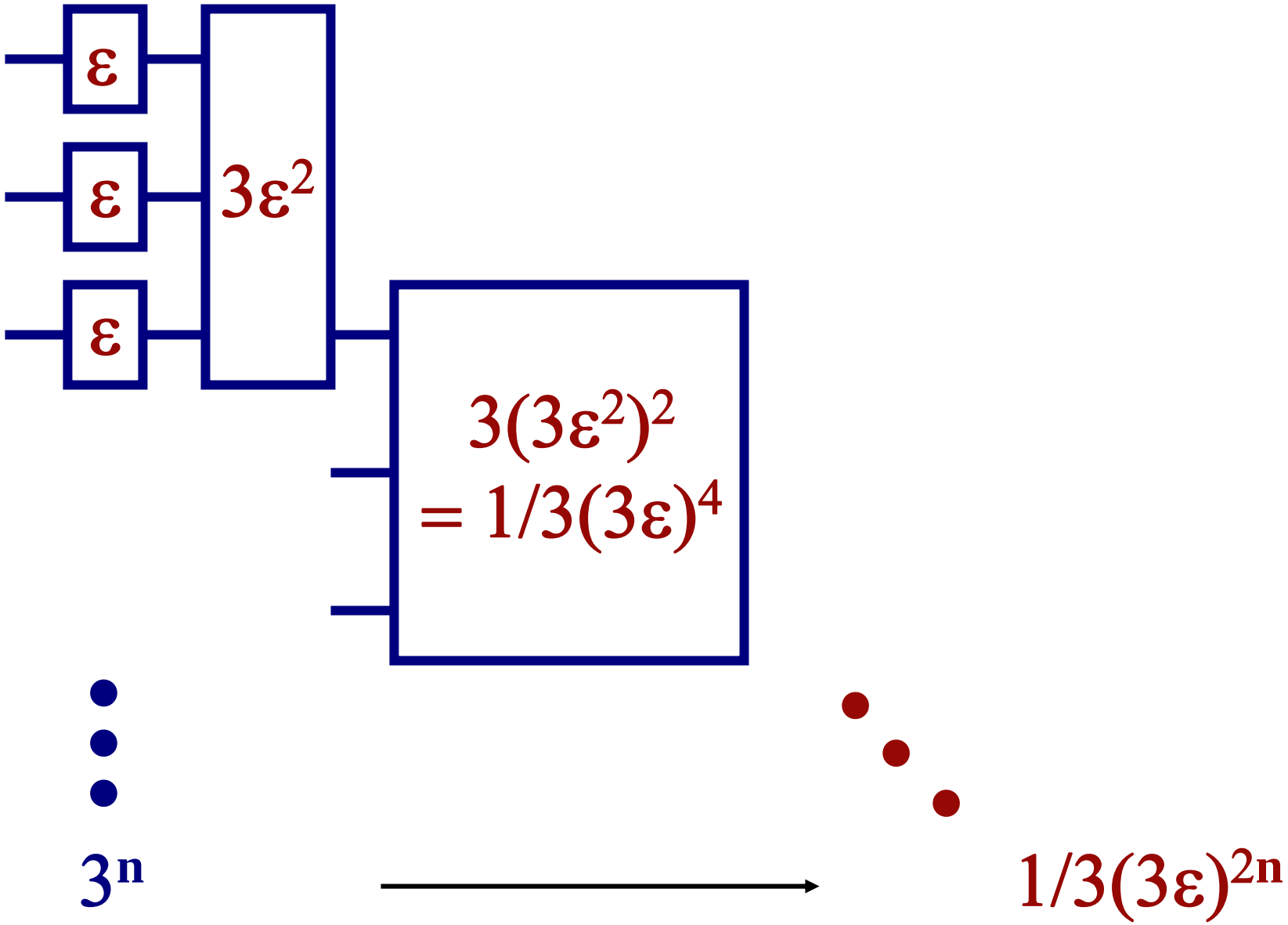
3'-5' proofreading exonuclease

http://www.med.upenn.edu/naf/services/catalog99.pdf

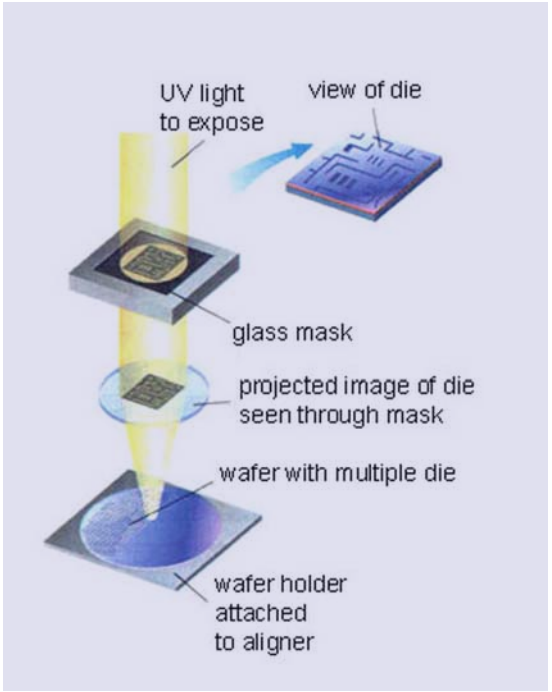
Beese *et al.* (1993), *Science*, **260**, 352-355.

http://www.biochem.ucl.ac.uk/bsm/xtal/teach/repl/klenow.html

Threshold Theorem



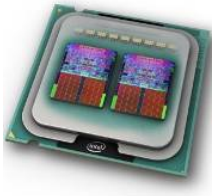
Conventional Fabrication (Optical Lithography)



- No error correction in individual transistor basis (> 40 mask steps)
- Complexity: Numerical aperture limits the structure size and density

http://www.fibics.com

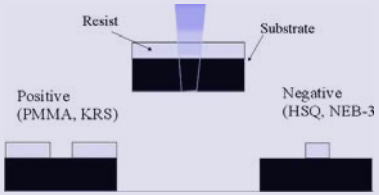
Fab-in-a-Box: Direct Write Nanocircuits



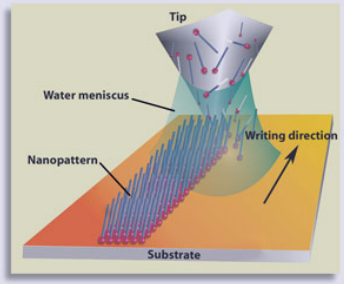
- Error correction at each transistor level
- Complexity: nanometer scale (above the conventional fab)

What are the methods?

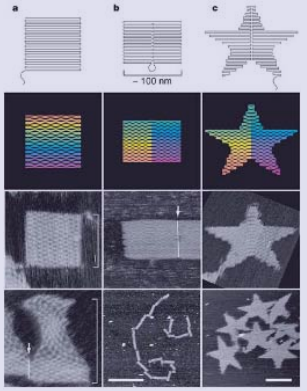
Electron Beam lithography



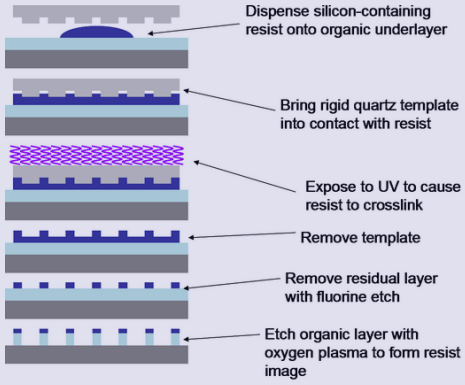
Dip-Pen Nanolithography



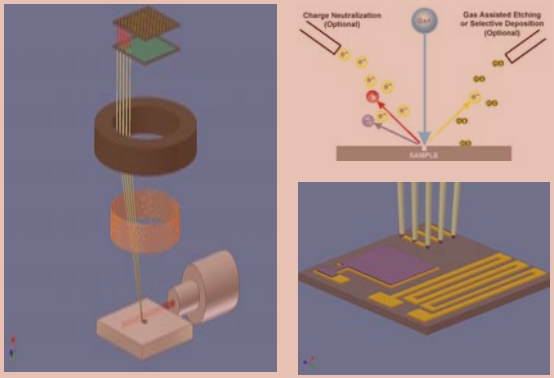
Self Assembly



Nanoimprint lithography



Focused Ion Beam



Direct imaging possible in each transistor level
→ Error correction

And others…..

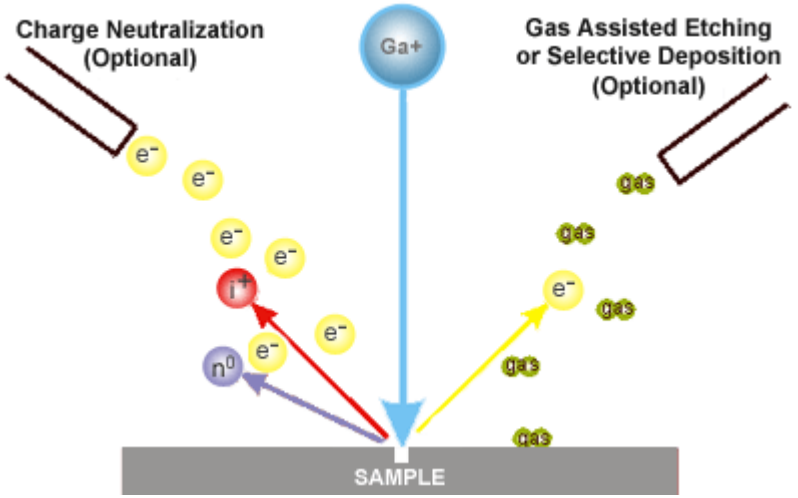
Focused Ion Beam (FIB)

FIB functions

1. Milling materials from a local area (~several nm)
2. Deposition of materials including Pt, SiO_2,etc.

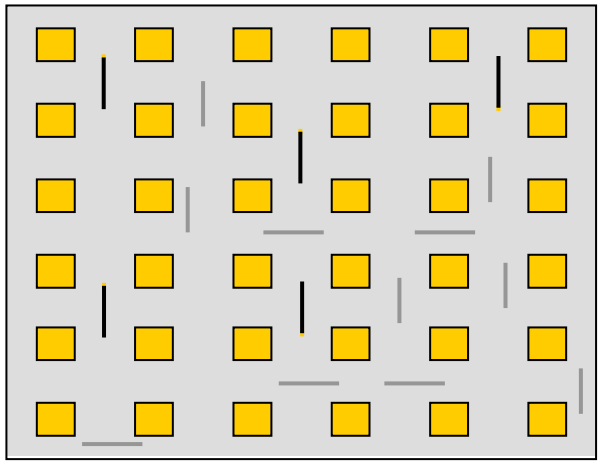
General Applications

1. Device modification (mask, pad, etc.)
2. TEM sample preparation
3. Section analysis
4. Direct write

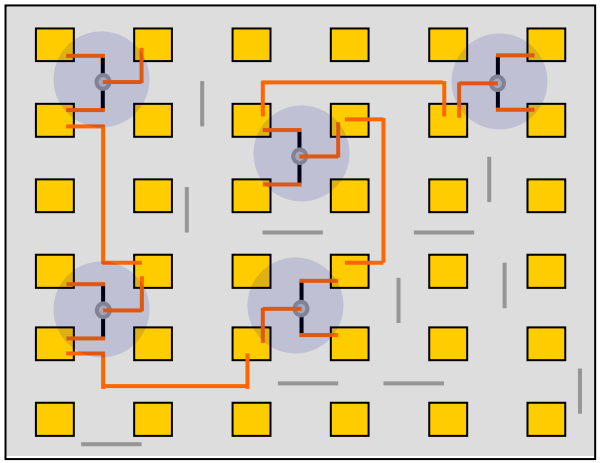


http://www.fibics.com

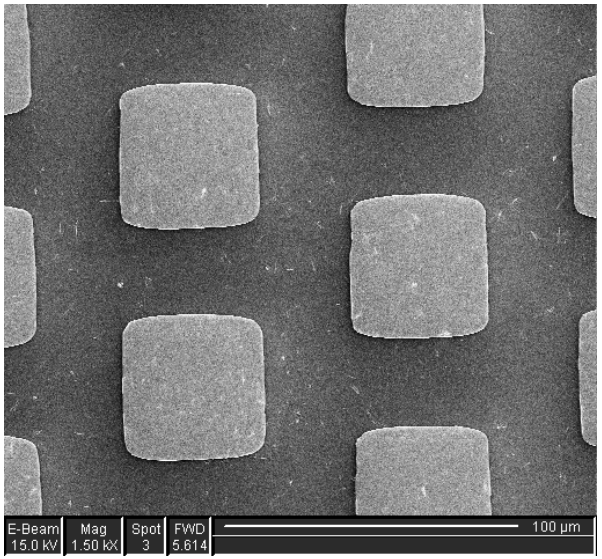
Prototype of error correction fabrication by FIB

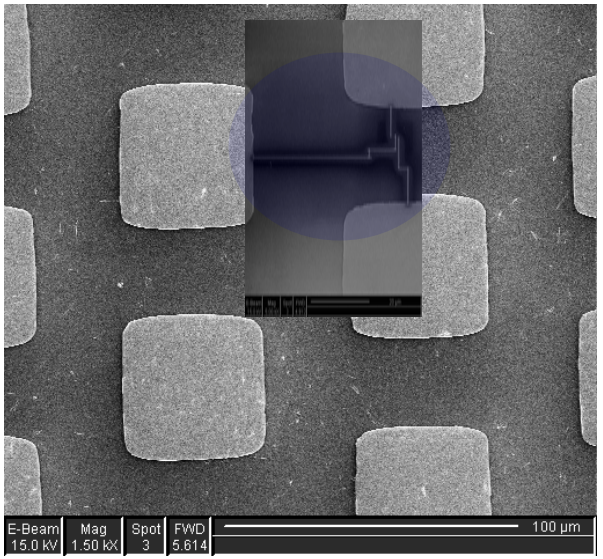


Extreme errors by random arrangement of nanowires

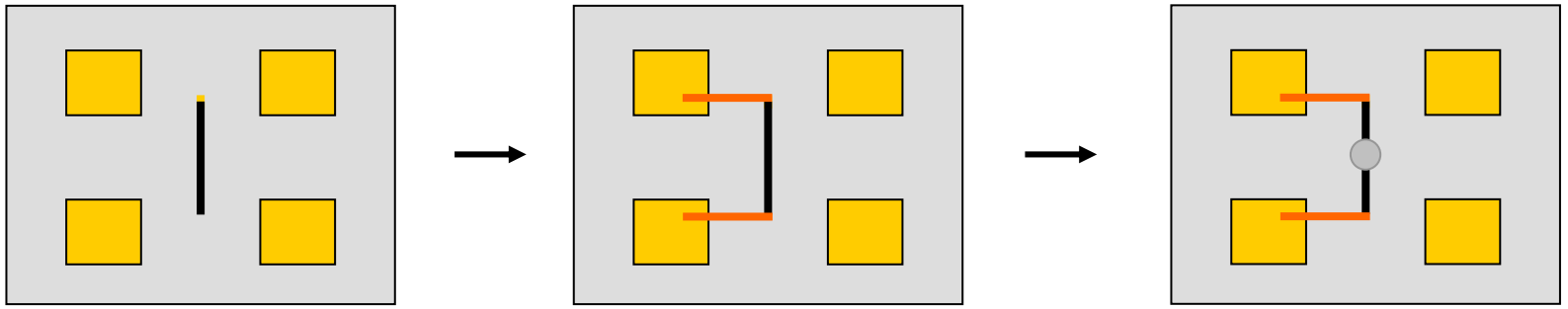


Transistor fabrication by error correction tool





Schematic of direct write Nanocircuits



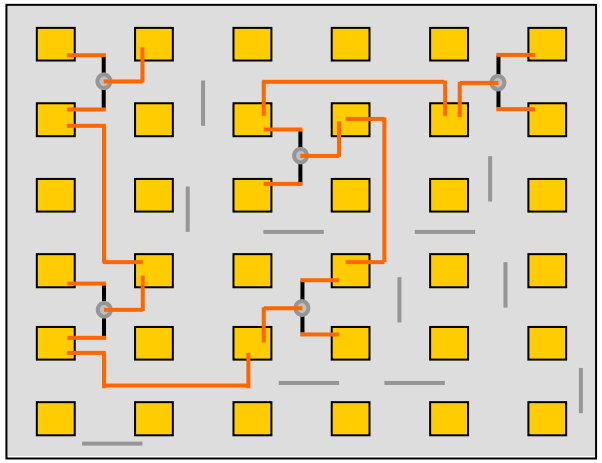
Randomly distributed semi-conducting Nanowire

FIB CVD Pt (source & drain)

FIB CVD SiO_2 (gate oxide)

FIB CVD Pt (gate electrode)

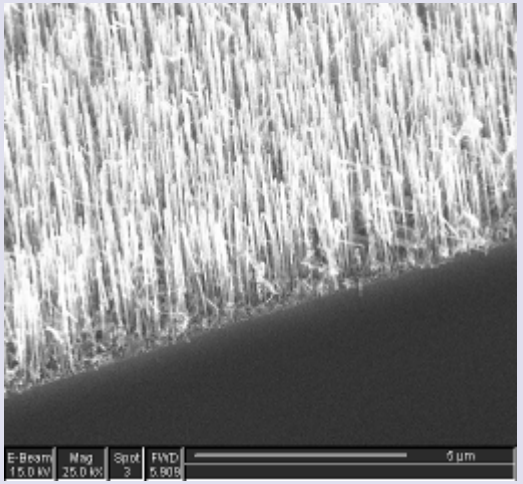
FET electrical Characterization



Large scale integration

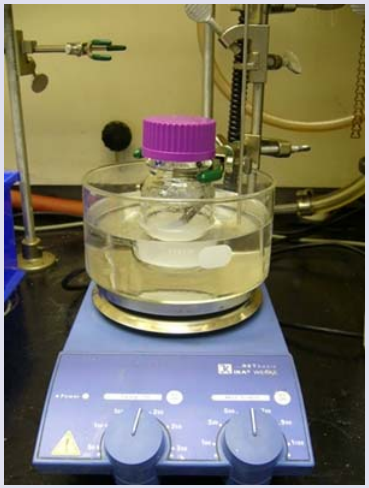
Detail: Nanowire Synthesis

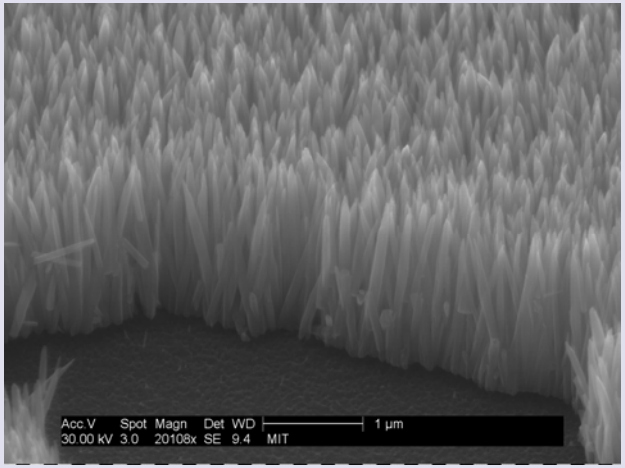
Gas phase
Nanowire synthesis:



Vapor-Liquid-Solid Mechanism (Si, GaN, etc.)

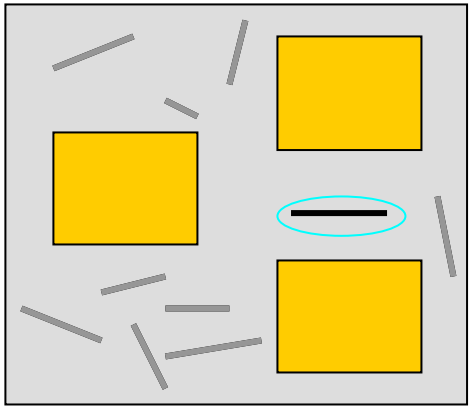
Liquid phase
Nanowire synthesis:



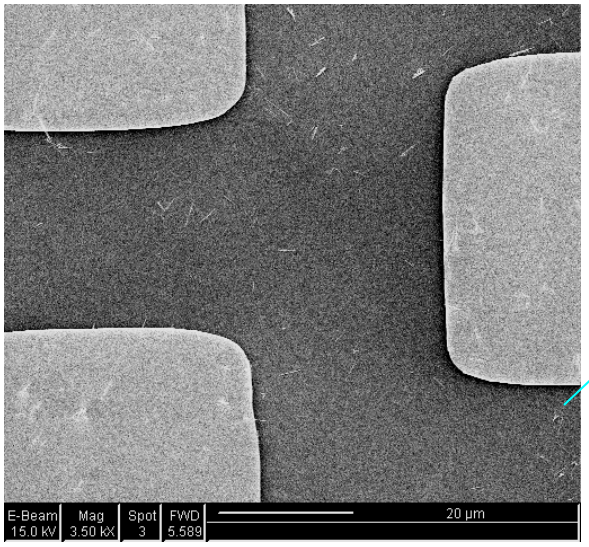


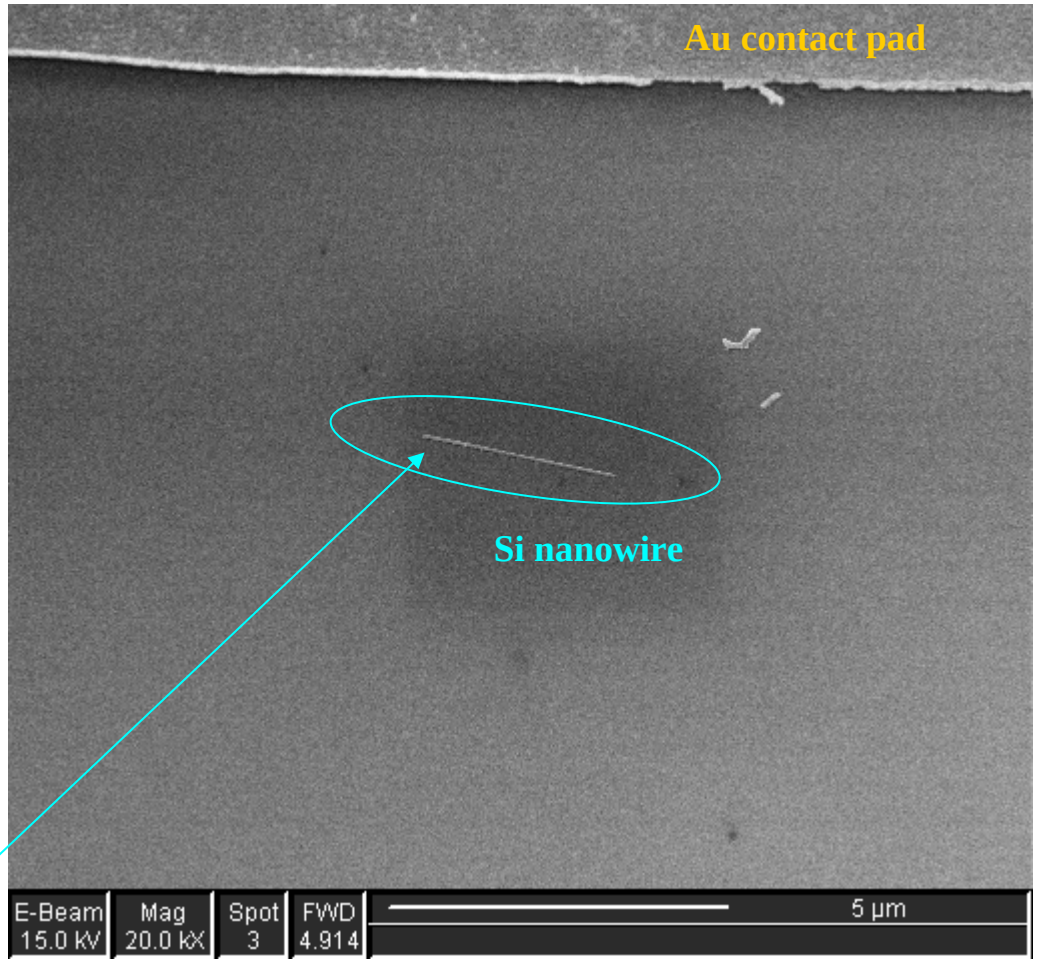
Supersaturation & heterogeneous growth (ZnO, $Cd(OH)_2$, ZnS, etc.)

Detail: Nanowire FET fabrication

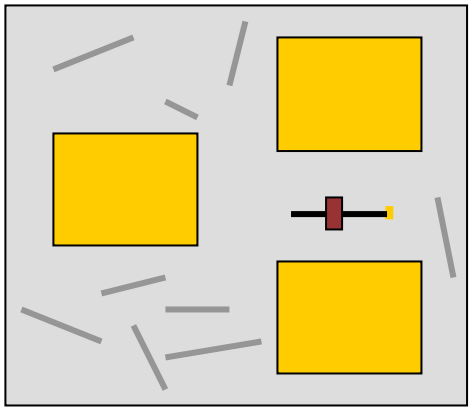


Selected Si nanowire

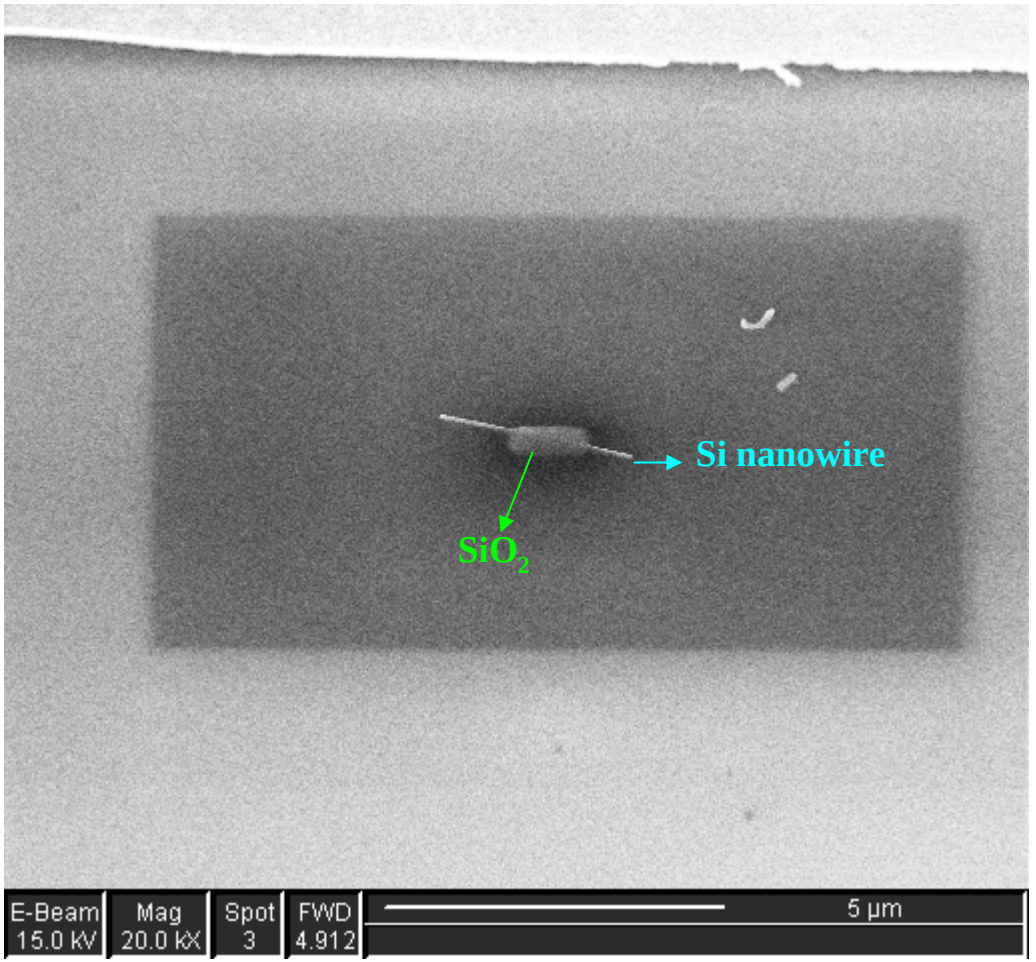




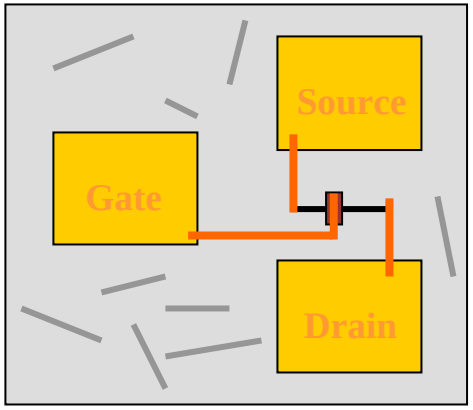
Detail: Nanowire FET fabrication



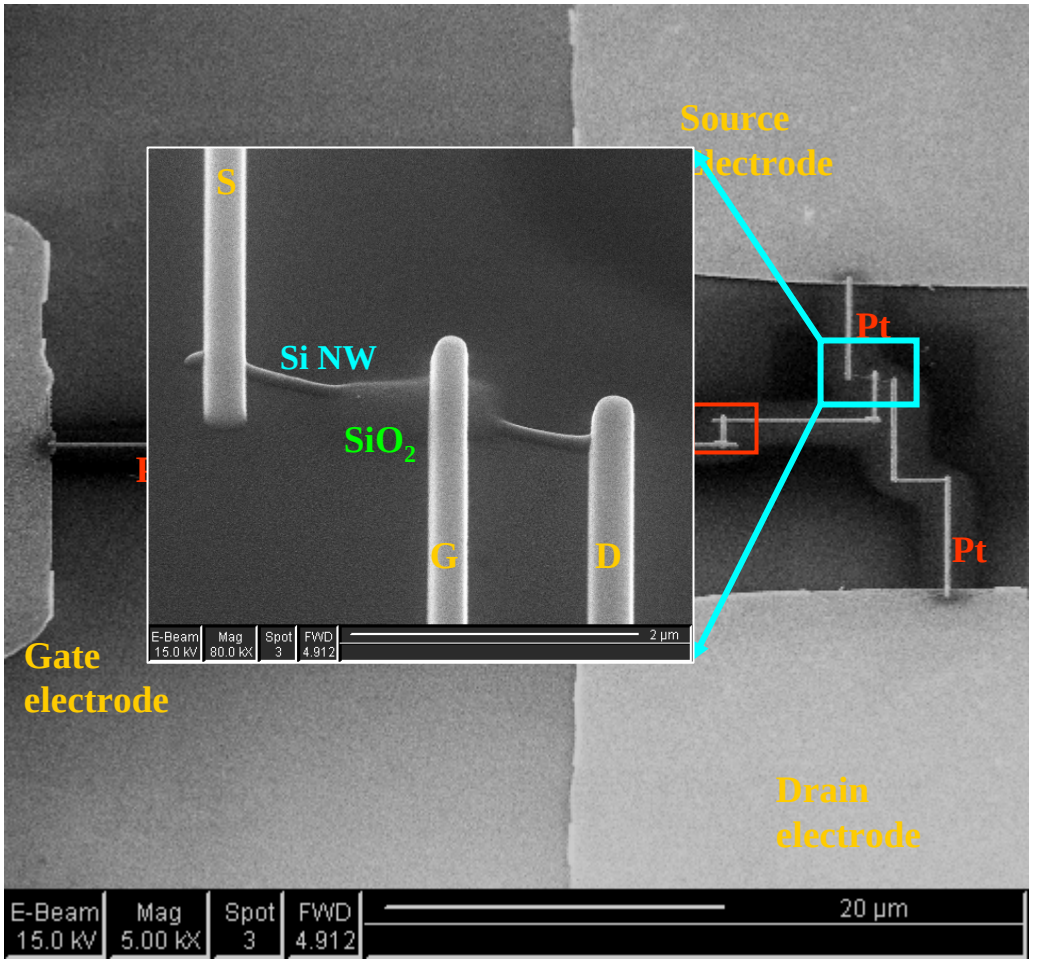
FIB CVD Gate oxide

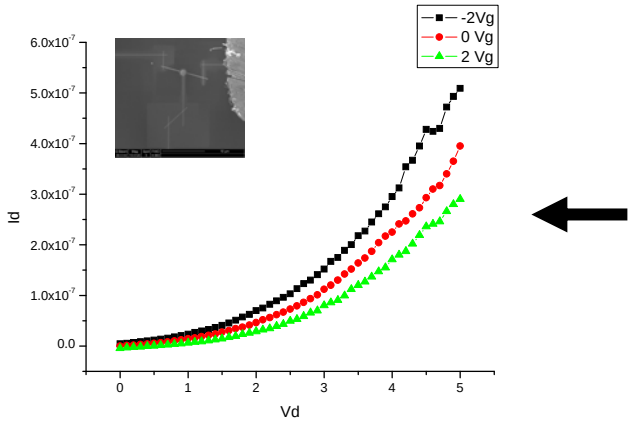


Detail: Nanowire FET fabrication



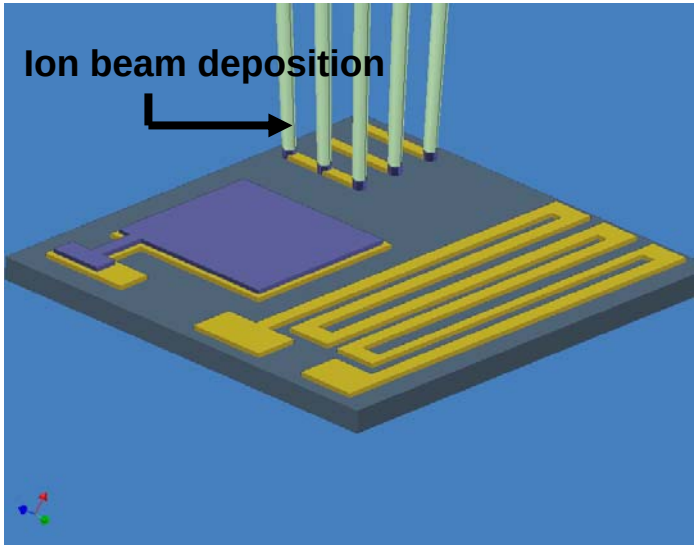
FIB CVD Pt wiring to each electrode





Depletion mode GaN FET

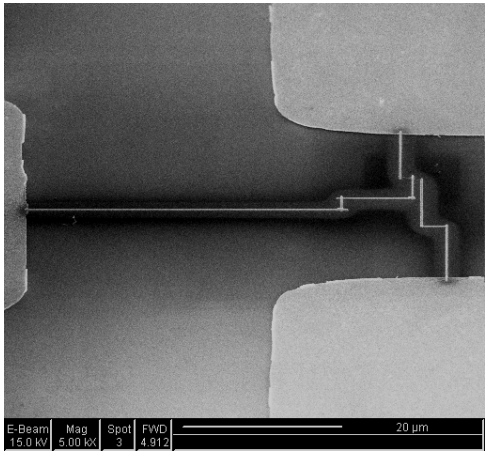
How to increase the speed of the fabrication?



< 20 nm Resolution

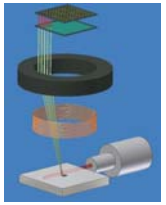
Novel 3 Dimensional Computer Architectures

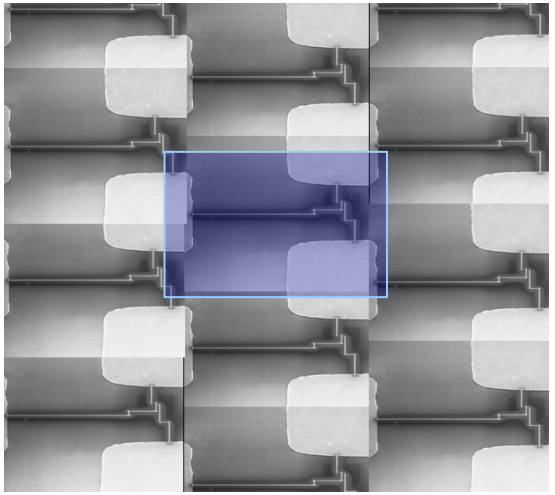
10^{12} Devices in << 24 hrs



Prototype circuit fabrication with error correction

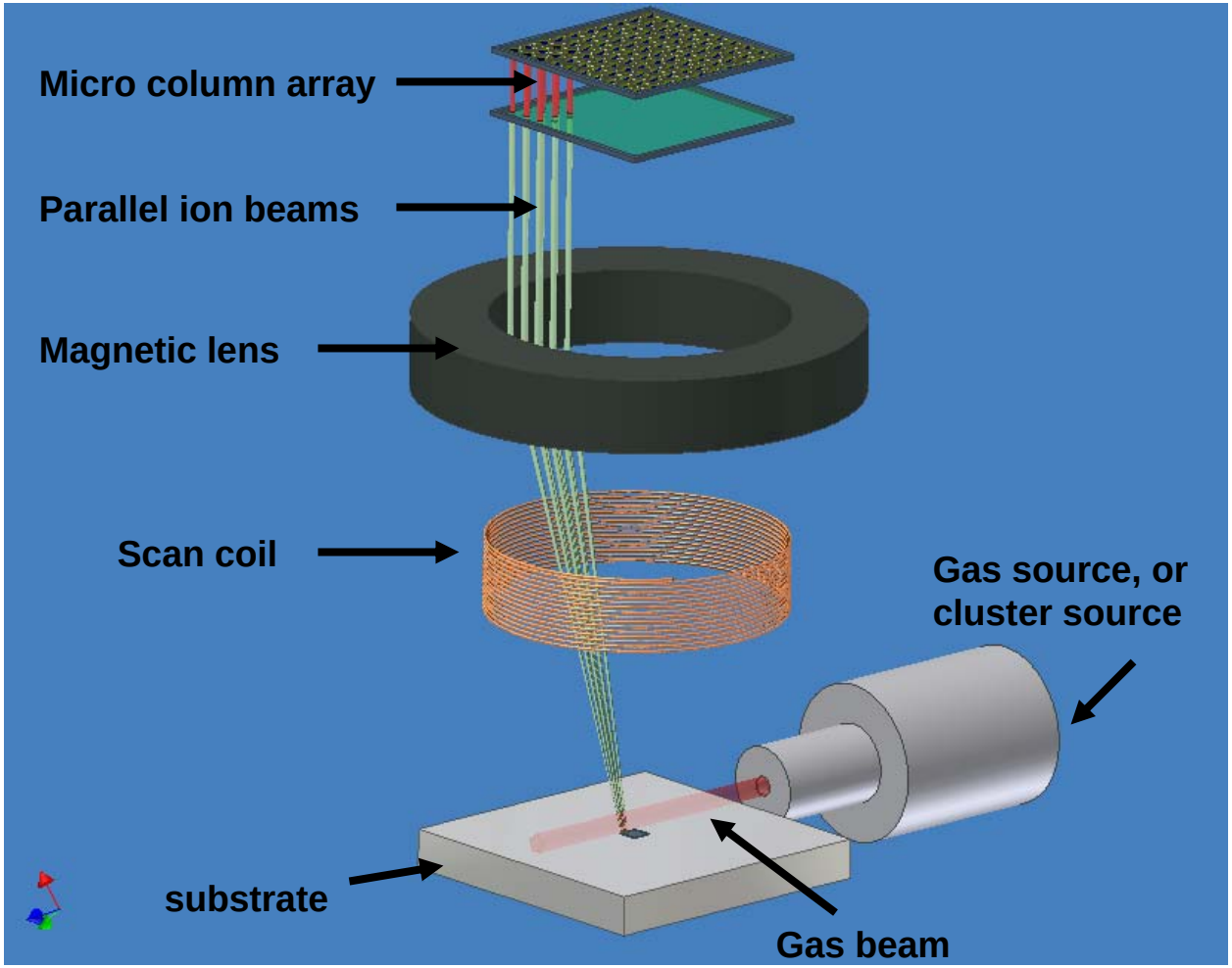
Parallel beam





Parallel Error Correcting Feedback Fabrication

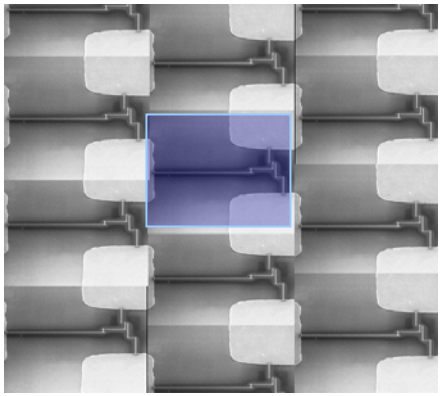
Parallel Focused Ion Beam (FIB)



Schematic of Moleographic Systems Showing Multiple Beam Fabrication with Feedback

Unique Features

- Ultrafast Highly Parallel Direct Fabrication
- On-The-Fly Molecular Scale Error Correction
- nm Inorganic Semiconductor Building Blocks

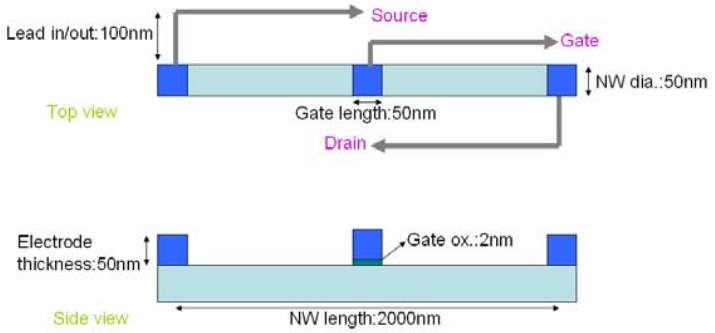


Other fabrication methods

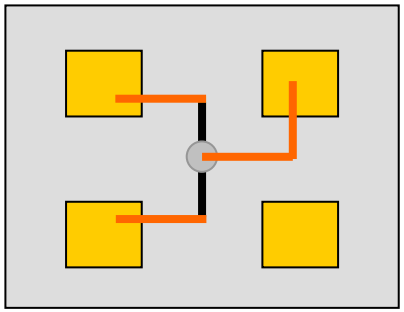
	Pre FIB process	FIB process	FIB volume (um^3) / transistor	FIB time(s)/ transistor	FIB time(s) /10^14 transistor	Cost($)/ transistor	Cost($) /400million transistors	Cost($)/ Avogadro number transistors
2D Whole device fabrication by FIB	None	Whole parts (Metal, Oxide, SC)	9.01E-01	5.41E-6	5.41E+08	8.59E-08	3.44E+01	8.59E+15
1D FIB assisted random nanowire circuit	VLS, solution nanowire synthesis	Interconnect oxides	1.50E-01	9.00E-07	9.00E+07	1.43E-08	5.72E+0	1.43E+15
1D FIB assisted DNA tile circuit	DNA tile synthesis	Interconnect	1.50E-01	9.00E-07	9.00E+07	1.43E-08	5.72E+0	1.43E+15
0D FIB assisted Nanowire synthesis and circuit fab	None	Catalysts (metal)	1.25E-04	7.50E-10	7.50E+04	1.19E-11	4.76E-03	1.19E+12

Assumption:

1. **One 1000 x 1000 multiple FIB beam**
2. **Design: simple MOSFET with 50nm gate**

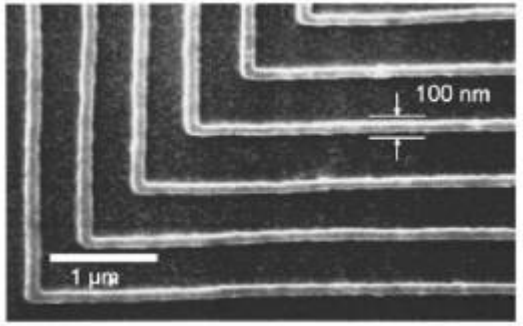


1. Whole device fabrication by FIB (2D)



FIB CVD parts

metal (source, drain, gate electrode)
oxide (gate)
Semiconductor (functioning part)



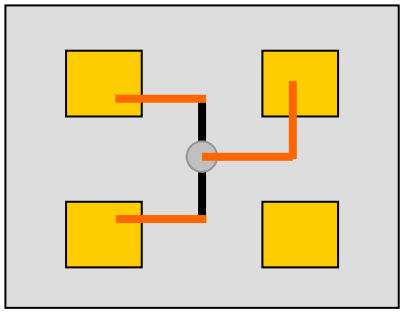
directly patterning organometallic nanoparticles
Wilhelm et al., 2004

FIB time(s)/ transistor	FIB time(s) /10^14 transistor	Cost($)/ transistor	Cost($)/ Avogadro number transistors
5.41E-6	5.41E+08	8.59E-08	8.59E+15

Requirement and issues

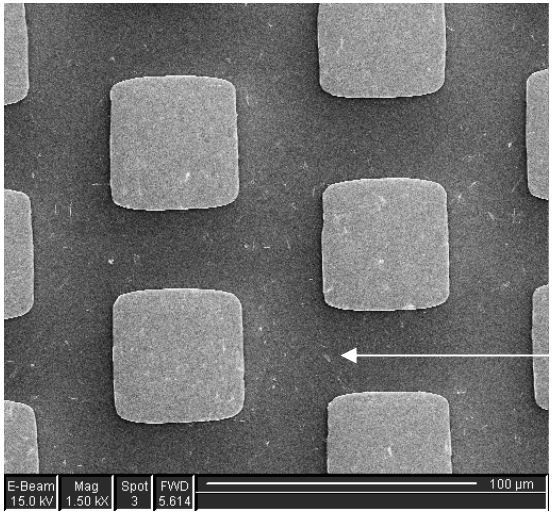
1. All metal CVD should be done in chamber
2. As transistor number increases, time for fabrication increase linearly
3. Too slow process

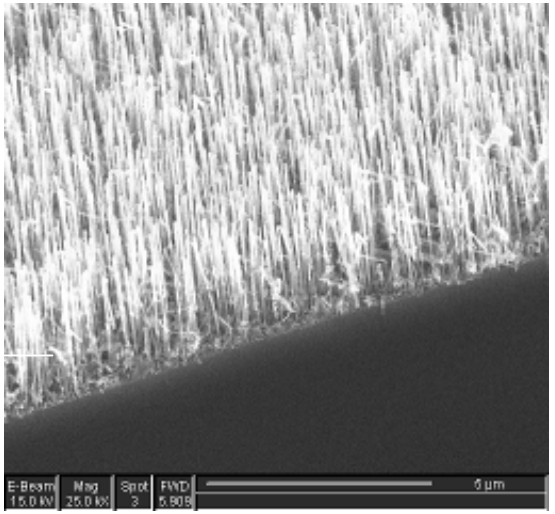
2. FIB assisted nanowire circuit (1D)



FIB CVD parts

metal (electrode wiring)
oxide (gate)





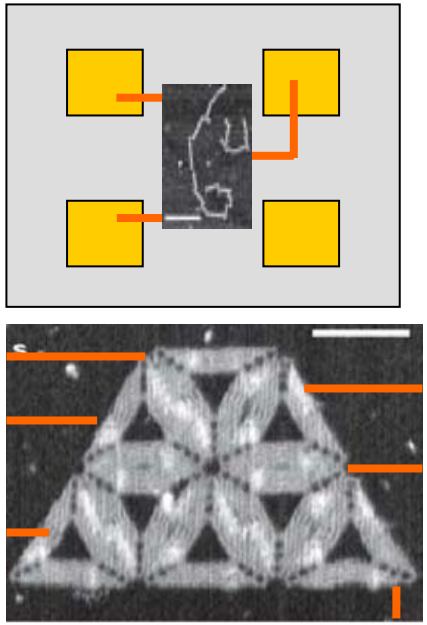
Parallel nanowire growth and random distribution of nanowires

FIB time(s)/ transistor	FIB time(s) /10^14 transistor	Cost($)/ transistor	Cost($)/ Avogadro number transistors
9.00E-07	9.00E+07	1.43E-08	1.43E+15

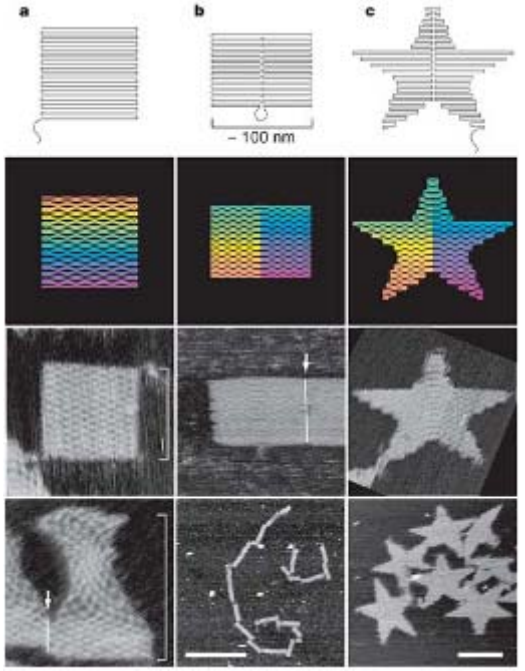
Requirement and issues

1. Once distributed nanowires are imaged, computer generates the mapping of each individual FET and fabricate multiple transistors

3. FIB assisted DNA tile circuit (1D)



FIB CVD parts
Metal wiring (to metal electrode)



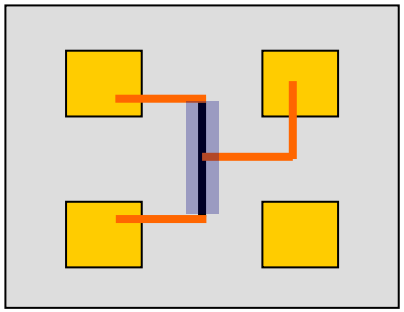
Folding DNA to create nanoscale shapes and patterns
Paul Rothemund, Nature 2006

FIB time(s)/ transistor	FIB time(s) /10^14 transistor	Cost($)/ transistor	Cost($)/ Avogadro number transistors
9.00E-07	9.00E+07	1.43E-08	1.43E+15

Requirement and issues

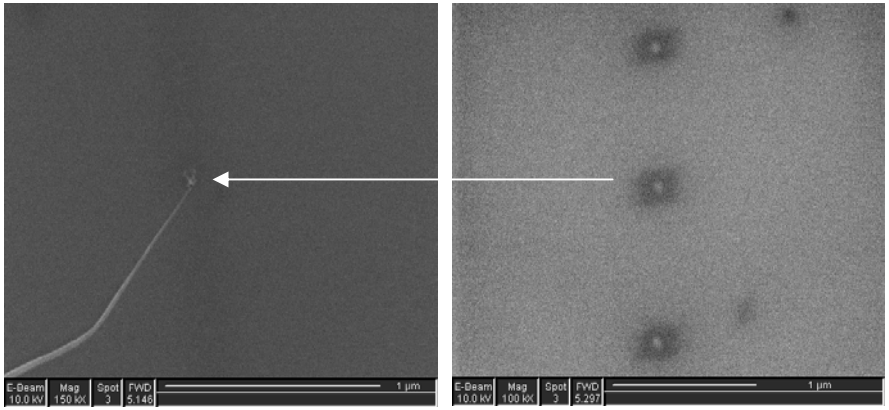
1. Would be preferable if DNA molecules are selectively assembled at desired location. (functionalization of surface, or stamping)

4. FIB assisted Nanowire synthesis and circuit fab (0D)



FIB CVD parts

metal catalyst
Oxide can be formed by heat treatment



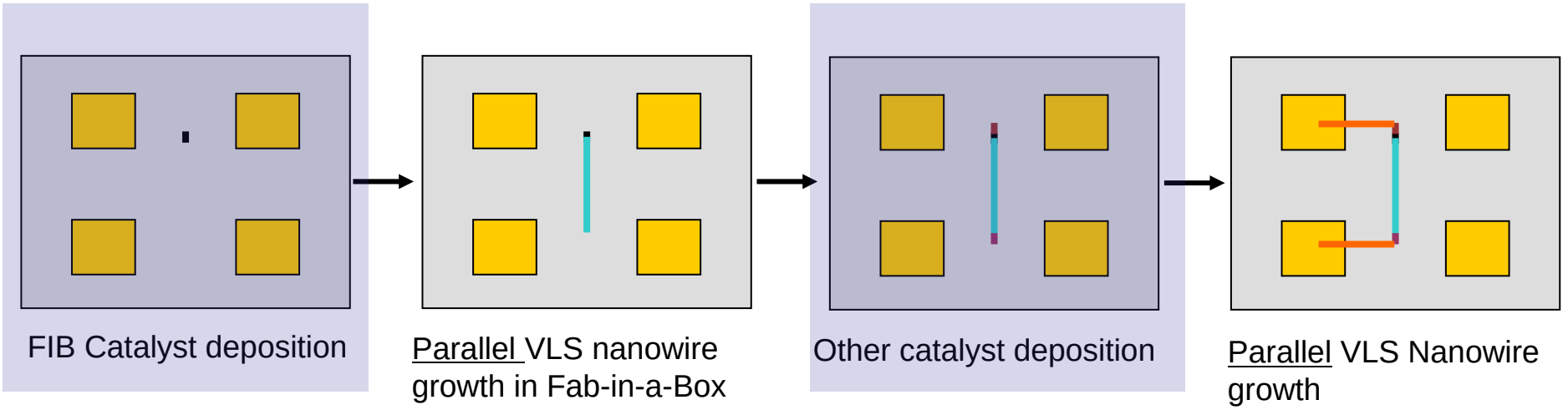
Kimin et al., unpublished

FIB time(s)/ transistor	FIB time(s) /10^14 transistor	Cost($)/ transistor	Cost($)/ Avogadro number transistors
7.50E-10	7.50E+04	1.19E-11	1.19E+12

Requirement and issues

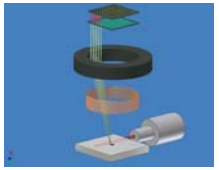
1. Planar nanowire synthesis required
2. Nanowire synthesis system should be compatible with Beam optics

4. FIB assisted Nanowire synthesis and circuit fab (0D)



Evaluation of methods

	Pre FIB process	FIB process	FIB volume (um^3) / transistor	FIB time(s)/ transistor	FIB time(s) /10^{14} transistor	Cost($)/ transistor	Cost($) /400million transistors	Cost($)/ Avogadro number transistors
2D Whole device fabrication by FIB	None	Whole parts (Metal, Oxide, SC)	9.01E-01	5.41E-6	5.41E+08	8.59E-08	3.44E+01	8.59E+15
1D FIB assisted Random nanowire circuit	VLS, solution nanowire synthesis	Interconnect oxides	1.50E-01	9.00E-07	9.00E+07	1.43E-08	5.72E+0	1.43E+15
1D FIB assisted DNA tile circuit	DNA tile synthesis	Interconnect	1.50E-01	9.00E-07	9.00E+07	1.43E-08	5.72E+0	1.43E+15
0D FIB assisted Nanowire synthesis and circuit fabrication	None	Catalysts (metal)	1.25E-04	7.50E-10	7.50E+04	1.19E-11	4.76E-03	1.19E+12



~20.8 hrs using single multiple FIB with error correction

Assumption:

1. **One 1000 x 1000 multiple FIB beam**
2. **Design: simple MOSFET with 50nm gate**

Complexity within 24hr with high precision (brain: ~10^{11} neurons,~10^{14} synapses)

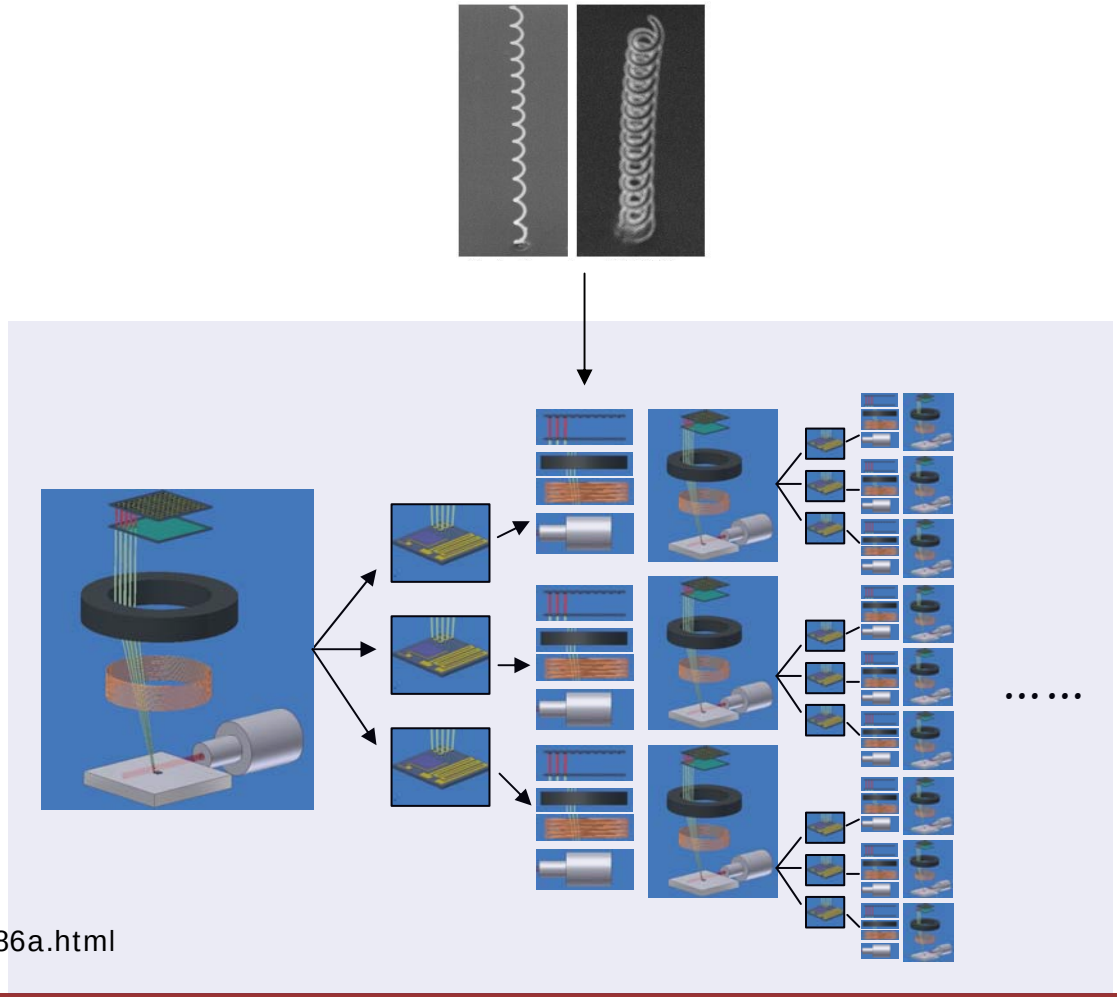
Error correction, and what else for the future Fab?

Another aspect of biology

→ Self replicating fabrication

Small scale machines

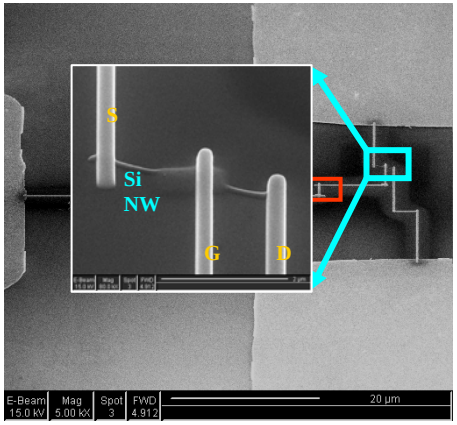
→ Scaling down the structure by making small scale three dimensional machines that can manipulate smaller scale objects.



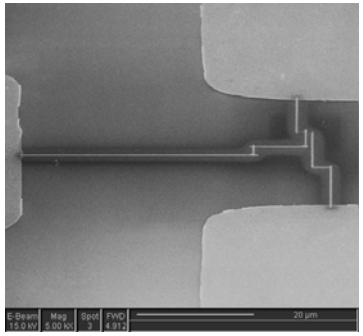
http://www.nanonet.go.jp/english/mailmag/2006/086a.html

Conclusion

- **Prototype Fab-in-a-Box Direct write nanowire circuit has been demonstrated with error correcting fabrication process.**



- **We are currently working on more complex circuit to boolean CA level.**



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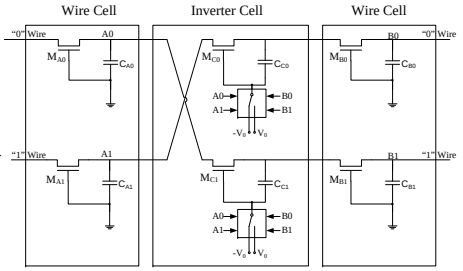

Any questions?